IN THE CLAIMS

Please amend claims 1, 3, 4, 9, 17, 18, 20, 25, 32, 33, 35, 37, 41, 42, 45, and 48 as follows:

1.   (CURRENTLY AMENDED) An adder for adding a signal at a first input *(A)* and a second input *(B)* to produce an adder output *(S)*, comprising:

a bypass input *(bypass)*; and

a logic circuit, communicatively coupled to the bypass input *(bypass)*, the first input *(A)*, and the second input *(B)*, the logic circuit configured to hold at least one of <u>a value of</u> the first input *(A)* and <u>a value of</u> the second input *(B)* according to the bypass input *(bypass)*.

2.   (ORIGINAL) The adder of claim 1, wherein the logic circuit further generates the adder output *(S)* without computing a new adder output according to the bypass input *(bypass)*.

3.   (CURRENTLY AMENDED) The adder of claim 1, further comprising:

a carry input *(C)* and a carry output *(CARRY)*; and

wherein the logic circuit further holds <u>a value of</u> the carry input *(C)* according to the bypass input *(bypass)*.

4.   (CURRENTLY AMENDED) The adder of claim 1, wherein the logic circuit further generates ~~the~~ <u>a</u> carry output *(CARRY)* without computing a new <u>adder</u> output according to the bypass signal *(bypass)*.

5.   (ORIGINAL) The adder of claim 1, wherein the logic circuit comprises a transmission gate adder.

-2-